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# Improving Bulk-Driven OTA Performance Using Cascode Differential Amplifier

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***Abstract*— This work presents a Bulk-Driven Operational Transconductance Amplifier (OTA) with a Telescopic Cascode Differential Amplifier, tailored for low-voltage and low-power analog applications such as biomedical signal processing. The bulk-driven input technique enables reliable operation at reduced supply voltages while improving linearity, making the design suitable for energy constrained environments. The telescopic cascode configuration enhances gain stability and frequency response, while additional features including PMOS active loads with current mirror action, a Class-AB output stage, and differential-to-single-ended conversion with gain boosting contribute to improved efficiency, stability, and bandwidth. The proposed design was simulated in Tanner EDA tools using a 45 nm CMOS process. Results confirm its effectiveness, achieving a DC gain of 45–50 dB, a gain-bandwidth product (GBW) of 2.5–3 MHz, and a phase margin of 70–75°, ensuring robust stability across operating conditions. Improvements in Common-Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR) are obtained through high-output-resistance cascode devices and enhanced tail biasing, which suppress noise and supply variations. The integration of a Class-AB output stage further improves slew rate, enabling efficient large-signal operation with minimal power overhead. These results demonstrate that combining bulk-driven input operation with cascode-based techniques provides an effective solution for high-performance, low-power OTA design. The proposed architecture is particularly well-suited for biomedical signal processing, where precision, noise immunity, and energy efficiency are critical design requirements.**

***Keywords*—**Operational Transconductance Amplifier (OTA), Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR).

## I. INTRODUCTION

The growing demand for energy-efficient and low-voltage analog circuit design has intensified the need for improved performance in core analog building blocks, especially in biomedical signal processing systems. Applications such as electrocardiography (ECG), electroencephalography (EEG), neural monitoring, and wearable healthcare devices require analog front-end circuits that can function accurately at low supply voltages while maintaining ultra-low power consumption, high gain, and robust noise immunity. The Operational Transconductance Amplifier (OTA) plays a central role in these systems; however, conventional gate-driven OTA architectures face challenges under such constraints, including limited input common-mode range, reduced transconductance, and poor performance at low supply voltages.

To address these issues, the bulk-driven technique has emerged as a promising approach. Unlike traditional designs that apply the input signal to the gate terminal of the MOS transistor, bulk-driven OTAs apply the signal to the substrate (bulk), enabling subthreshold operation and expanding the input dynamic range. This makes them ideal for ultra-low voltage environments, especially in battery-operated biomedical devices. Nevertheless, bulk-driven OTAs inherently suffer from drawbacks such as lower DC gain, degraded Common-Mode Rejection Ratio (CMRR), limited Power Supply Rejection Ratio (PSRR), and increased noise sensitivity.

To overcome these limitations, this work introduces an enhanced OTA architecture that combines the benefits of bulk-driven input with a cascode differential amplifier—specifically, a telescopic cascode configuration. This approach boosts output resistance and transconductance, significantly improving DC gain, CMRR, PSRR, and bandwidth while preserving low power operation. Designed in 180nm CMOS technology and simulated using Synopsys tools, the proposed design shows considerable performance improvements over traditional OTA topologies.

The significance of this work lies not only in its technical innovation but also in its potential impact on biomedical electronics. By enhancing key performance metrics critical for signal integrity such as gain, noise rejection, and power efficiency the proposed OTA addresses the unique challenges of analog front-end design in life-critical biomedical systems. This hybrid design thus serves as a compelling solution for advancing the performance of analog circuits in modern, energy-constrained medical applications.

In addition, the bulk-driven approach provides a wider input common-mode range**,** ensuring robust operation even with weak bio-signals. The telescopic cascode structure contributes to improved frequency response and enhanced stability**,** making the design suitable for high-fidelity biomedical signal amplification.

## II. LITERATURE REVIEW

The design of low-voltage, energy-efficient operational transconductance amplifiers (OTAs) remains a critical research area in analog and mixed-signal circuit design, especially for applications like biomedical signal processing, where low power and high precision are essential. Grasso et al. [1]

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provided a comprehensive theoretical framework for single Miller capacitor compensation techniques. Their study systematically compared several frequency compensation methods, offering key insights into phase margin optimization and bandwidth enhancement. This foundational analysis supports designers in selecting appropriate compensation strategies tailored to specific OTA architectures.

Kulej et al. [2] introduced a 0.3 V rail-to-rail OTA based on a bulk-driven differential input stage, fabricated using 0.13 µm CMOS technology. This design demonstrated high linearity across the entire input common-mode range, addressing the traditional dead-zone issue found in gate-driven topologies. The bulk-driven input, combined with an optimized layout, delivered improved power efficiency and robustness in ultra-low-voltage conditions.

A notable contribution by Centurelli et al. [3] proposed an ultra-low-voltage Class-AB OTA leveraging a localized common-mode feedback (CMFB) mechanism and body-to-gate biasing interface. This configuration enhanced both the output swing and linearity while maintaining sub-0.5 V operation. The topology is particularly beneficial for analog front-end designs in biomedical instrumentation, where high signal integrity is essential.

Woo and Yang [4] developed a 0.25 V three-stage rail-to-rail OTA incorporating an NMOS gate-driven stage within a traditional bulk-driven amplifier. Their use of asymmetric self-cascode transistors and indirect feedback compensation significantly increased DC gain and improved unit-gain bandwidth. The multi-stage configuration effectively addressed gain limitations typically associated with bulk-driven designs.

In a related study, Abdelfattah *et al.* [5] developed an ultra low-voltage CMOS self-biased operational transconductance amplifier (OTA) featuring a rail-to-rail input range. This configuration ensures high reliability, improved linearity, and reduced power consumption, making it highly suitable for low-voltage, low-power analog and mixed-signal circuit applications such as portable and biomedical systems.

Finally, Ballo et al. [6] reported a compact single-stage bulk-driven OTA operating at 0.4 V and consuming only 81.3 nA. By enhancing the transconductance through topology-level improvements, the design achieved respectable performance while maintaining design simplicity—ideal for ultra-low-power portable electronics.

## II. METHODOLOGY

### 1. Existing Methodology

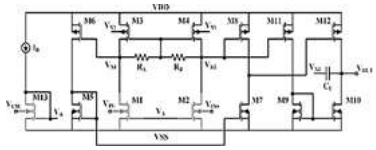

Fig. 1.1 Bulk driven OTA

The existing diagram of bulk driven OTA as shown in Fig.1.1. The proposed work focuses on enhancing the performance of a bulk-driven operational transconductance amplifier (OTA) by incorporating a telescopic cascode differential amplifier at the input stage. This approach aims to address the limitations of conventional bulk-driven OTAs, particularly the low transconductance, reduced DC gain, and moderate rejection ratios, while preserving the advantages of ultra-low-voltage operation. The input stage employs bulk-driven transistors to enable rail-to-rail input functionality under low supply voltages, while the telescopic cascode configuration increases the output resistance and suppresses gain degradation. Local positive feedback is introduced through cross-coupled bulk–drain connections in the load devices, effectively boosting the equivalent bulk transconductance without significantly increasing power consumption.

The second stage provides additional gain amplification, ensuring that the signal is sufficiently strengthened before reaching the output driver. A class-AB output stage is implemented with adaptive biasing, enabling the circuit to deliver higher load currents during dynamic operation while maintaining a low quiescent current in steady state. This improves the slew rate and load-driving capability without compromising energy efficiency. The biasing network is realized using Wilson current mirrors to ensure accurate and temperature-stable bias currents across all stages.

For frequency stability, a single Miller compensation capacitor is connected between the output node and the intermediate stage. This technique reduces silicon area, simplifies the compensation network, and maintains a high gain–bandwidth product. The transistor dimensions and bias currents are carefully selected to maximize bulk transconductance in the input pair, optimize phase margin, and ensure operation under process and temperature variations. Simulations are carried out using Tanner EDA T-Spice in 180-nm CMOS technology, including DC, AC, transient, and noise analyses, as well as corner and Monte Carlo evaluations. The methodology is designed to achieve a higher DC gain, improved CMRR and PSRR, increased slew rate, and enhanced gain–bandwidth performance compared to conventional bulk-driven OTAs, while retaining a compact layout and low-power operation.

### 2. Proposed Methodology

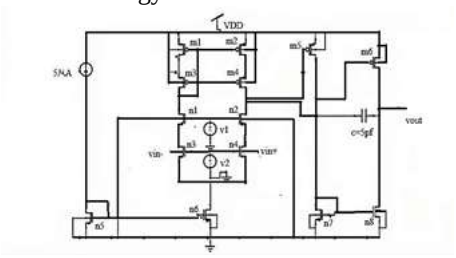

Fig 2.1 proposed OTA

The simplified schematic of the proposed OTA is depicted in fig. 2.1. The proposed OTA employs a bulk-driven NMOS differential pair (n3–n4) as the input transconductor, where the input signals Vin+ and Vin− are applied to the body terminals while the gates are biased at a fixed potential $V_A$ (represented by bias nodes $v_1$ and $v_2$). Above this pair, NMOS devices m3–m4 act as telescopic cascodes, which maintain the input



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transistors in saturation and significantly increase the output resistance at internal nodes $n_1$ and $n_2$. The PMOS pair m1–m2 serves as active loads, forming a current mirror connected to $V_{DD}$, thereby contributing to differential-to-voltage conversion. A biasing network provides the necessary current reference, where a 5 µA source drives current mirrors and the transistor n6 acts as the tail current sink to ensure proper differential operation. For single-ended conversion and additional gain boosting, the right-hand branch with transistors m5 and m6 translates the differential currents into a single-ended voltage at the output node $v_{out}$. To enhance large-signal performance, the output stage incorporates transistors n7–n8, which act as a dynamic return path, providing class-AB or AB-lite behavior depending on the biasing, thus improving slew rate and output stability. Finally, a compensation capacitor Cc=5 pF is connected between the internal high-gain node and the output to establish a dominant pole, ensuring stability and achieving the desired phase margin.

*2.1 Bulk-driven input pair (n3, n4, tail n6)*

The differential input is applied to the body (bulk) terminals of transistors n3 and n4, while their gates are held at a fixed bias $V_A$. A tail current source n6 provides the total tail current $I_{tail}$, which divides into the two branches as $I_D \pm \Delta I_D$ according to the applied differential body voltage. The incremental differential input $v_{id}$ is defined as.

$$Vid = V_{in+} - V_{in-}$$

The relevant small-signal transconductance for a bulk-driven device is the *body* transconductance $g_{mb}$ , which is related to the gate transconductance $g_m$ by

$$g_{mb} = \eta g_m \text{ ,with } 0.1 \lesssim \eta \lesssim 0.4,$$

where $\eta = \partial V_T / \partial V_{SB}$ is the body-effect coefficient (technology dependent). Using the usual expression for gate transconductance in strong inversion

$$gm \approx 2ID/V_{ov}$$

The amplifier common-mode gain $A_{cm}$ is strongly influenced by the tail impedance $r_{o,tail.}$ Increasing the tail impedance (for example, by using a cascode or Wilson tail current source) reduces the common-mode gain and therefore improves the common-mode rejection ratio:

$$CMRR = A_d / A_{cm},$$

usually expressed in dB as $20\log_{10}(A_d/A_{cm})$. In practice:
raising $r_{o,tail} \Rightarrow A_{cm} \Rightarrow$ increases CMRR.
improving per-branch output resistance $R_{o,branch}$ (via cascodes) $\Rightarrow$ raises differential gain $Ad \approx g_{mb} R_{o,branch} \Rightarrow$ further improves CMRR.

2.2 Telescopic NMOS cascodes (m3, m4) and internal nodes (n1, n2)

The NMOS cascode transistors (m3, m4) placed above the input pair (n3, n4) maintain the input transistors in saturation the internal nodes n1 and n2. This telescopic cascode arrangement therefore multiplies the small-signal output resistance and raises the stage gain while isolating the input transistors from large variations at the output.

Consider the lower device (input transistor) with small-signal output resistance $r_o$,$n_3$ and the cascode device m3 with transconductance $g_{m,m3}$ and output resistance $r_{o,m3}$. The effective output resistance seen at node n1 (the drain of m3) is approximately

$$R_{o,low} \approx r_{o,n3}(1 + g_{m,m3} r_{o,m3})$$

This expression shows that the cascode multiplies the intrinsic output resistance by the gain factor $1+g_{m,m3}\ r_{o,m3}$. If both the lower and cascode devices have substantial intrinsic resistance, telescoping multiple stages multiplies these factors and yields very large overall $R_{o.}$

The small-signal voltage gain from the input transconductor to the internal high node (before the PMOS load) for one branch

$$A_{branch} \approx g_{mb} R_{o,branch}$$

where $g_{mb}$ is the bulk-driven transconductance of the input transistor and $R_o$, branch is the total output resistance seen by the transconductance source (including the cascode multiplication). Increasing $_{Ro,}$branch therefore directly raises the differential-stage gain.

Raising the output resistance increases the dominant pole's time constant when combined with node capacitances. The pole at the internal node $p_1$ can be approximated by

$$p1 \approx 1/R_{obranch}\ C_n$$

where $C_n$ is the total capacitance at the internal node (parasitic + Miller contribution). A larger $R_o$ shifts $p_1$ to lower frequency, which must be compensated by choosing the Miller capacitor Cc and second-stage transconductance appropriately to preserve phase margin.

To ensure that both the input transistors (n3, n4) and their cascodes (m3, m4) remain in saturation over the required input common-mode range, the available supply headroom must satisfy:

$$V_{CM,in} + V_{OV,n3} + V_{DSsat,m3} + V_{DSsat,PMOS\ load} < VDD,$$

where

and substantially increase the effective output resistance seen at

- $V_{CM,in}$, is the input common-mode voltage,
- $V_{OV,n3} = V_{GS,n3} - V_{T,n3}$ is the overdrive of the input transistor,
- $V_{DSsat,m3}$ is the minimum $V_{DS}$ to keep the cascode m3 in saturation, and
- $V_{DSsat,PMOS\ load}$ is the minimum $V_{SD}$ (for PMOS load) required for its saturation.
- This inequality sets a practical constraint on bias levels and device sizing: if the left-hand sum approaches $V_{DD}$, one or more devices will leave saturation, degrading gain and linearity.

*2.3 PMOS active loads / mirror (m1, m2)*

The PMOS active loads m1 and m2 convert the differential branch currents at internal nodes $n_1$ and $n_2$ into voltages and, when arranged as a current mirror, optionally replicate one


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branch current to form a single-ended output. As active loads, these PMOS transistors provide a high small-signal load resistance while allowing adjustable bias currents through current-mirror ratios.

For a long-channel PMOS device biased in saturation, the small-signal output resistance is approximately the transistor's intrinsic $r_o$ . Using longer channel length L for the load transistors increases $r_o$ (reducing channel-length modulation), so designers commonly select long-L devices for the loads:

$$R_{o,load} \approx r_{o,PMOS} (\text{use long } L \Rightarrow r_o \uparrow).$$

When the gates of m1 and m2 are driven from a cascode current mirror (i.e., the mirror that drives their gates includes cascode transistors), the effective output resistance seen into the load node increases substantially. A cascode mirror boosts mirror output resistance approximately by the factor $1+g_m r_o$ of the added cascode device. Thus, a cascode-biased load yields.

$$R_{o,load,eff} \uparrow \sim r_{o,PMOS}(1+g_{m,cas}\, r_{o,cas}).$$

Because the load node is now less sensitive to changes in $V_{DD}$, the coupling from supply fluctuations into internal nodes n1/n2 is reduced, improving low-frequency PSRR. In other words, raising $R_{o,load}$ reduces the transfer function from $V_{DD}$ to the output node and increases PSRR in dB.

Combining the transconductance and load resistance gives the per-branch small-signal voltage gain to the internal node:

$$A_{branch} \approx g_{mb}(R_{o,low} \| R_{o,load})$$

If $R_{o,load} \gg R_{o,low}$ , the branch gain is limited by $R_{o,low}$ ; conversely, when the load dominates, the PMOS load sets the gain.

*2.4 Differential-to-single-ended conversion & second gain (m5, m6)*

Transistor m5 senses one internal high-impedance node (for example $n_1$ or $n_2$) and converts the local differential branch voltage/current into a current or voltage that drives the next stage. Transistor m6 forms the mirror/load and completes the conversion, producing the single-ended output $v_{out}$. Practically, the m5–m6 path implements a second gain stage whose small-signal transconductance and load resistance determine the second-stage gain and the final single-ended output amplitude. the second-stage small-signal transconductance as

$$gm2 \equiv gm,(m5/m6\ path),$$

which, for a MOSFET biased in strong inversion, can be approximated by

$$g_{m2} \approx 2I_{D2} / V_{ov2}$$

where $I_{D2}$ is the DC bias current through the m5/m6 path and $V_{ov2}$ the overdrive voltage of the sensing/device pair

A small differential current $i_d$ generated by the input transconductor produces a differential voltage at the internal node:

$$V_n \approx i_d\, (R_{o1} \| R_{o,load}),$$

where $R_{o1}$ is the telescopic output resistance of the first stage and $R_{o,load}$ the PMOS load resistance. Transistor m5 senses $v_n$ and produces a small-signal current $i_5 = g_{m2}\, v_n$ that is mirrored/converted by m6 into the single-ended output $v_{out}$ across the output resistance $R_{o2}$.

The voltage gain of the second (single-ended) stage is

$$A2 \approx g_{m2}\, R_{o2},$$

where $R_{o2}$ is the resistance seen at the second-stage or output node (including the output device's $r_o$, any load, and the effect of bias mirrors).

Viewing the amplifier as two cascaded stages (input differential stage → second single-ended stage), the low-frequency open-loop gain is approximately the product of the two per-stage gains:

$$A0 \approx g_{mb}\, R_{o1\_} \times g_{m2}\, R_{o2}$$

where:

$g_{mb}$ is the bulk transconductance of the input device (stage 1),

$R_{o1}$ is the effective output resistance at the internal node (telescopically increased by cascodes),

$g_{m2}$ and $R_{o2}$ are as defined above.

This factorization highlights that improving either stage (larger where:

$g_{mb}$ is the bulk transconductance of the input device (stage 1),

Ro1R_{o1}Ro1 is the effective output resistance at the internal node (telescopically increased by cascodes),

$g_{m2}$ and $R_{o2}$ are as defined above.

This factorization highlights that improving either stage (larger $g_{mb}$ or $R_{o1}$; larger $g_{m2}$ or $R_{o2}$) raises the overall DC gain.

When a Miller compensation capacitor Cc is placed between the internal high-gain node and $v_{out}$, the dominant pole and the GBW can be approximated (single-dominant-pole assumption) as:

$$GBW \approx g_{m2}/2\pi Cc\ ,$$

provided the stage-2 transconductance and the Miller connection dominate the loop dynamics. The dominant pole frequency is roughly

$$p_1 \approx 1 / 2\pi Ro2Cc.$$

(with more accurate multi-pole expressions including the internal node capacitances and $R_{o1}$ ). The internal node pole supported by $R_{o1}$ and its capacitance $C_n$ is

$$p_n \approx 1 / 2\pi R_{o1} C_{n1}$$

Design of Cc and of $g_{m2}$ must ensure adequate phase margin (typ.60deg−75deg) when combined with the load capacitance $C_L$.

*2.5 Class AB path (n7,n8)*

The auxiliary transistors n7 and n8 form a *Class-AB-lite* output return path. Their role is twofold:

To provide additional sourcing and sinking current during transient conditions, thereby improving the slew rate of the amplifier.

To stabilize the DC output common-mode level, ensuring the output remains within the desired operating range for proper signal swing and load driving capability.

By automatically activating when large signal transitions occur, this Class-AB-lite path supplements the steady bias current with extra current drive, without continuously consuming large amounts of static power.

The slew rate (SR) quantifies the maximum rate of change of the output voltage. With load capacitance $C_L$ (including both the external load and the Miller compensation capacitor reflected at the output), the upward and downward slew-rate limits are:



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$SR\uparrow \approx I_{source} / C_L$, $SR\downarrow \approx I_{sink} / C_L$.

$I_{source}$ is the maximum current supplied to charge $C_L$ during a rising output transition.

$I_{sink}$ is the maximum current discharged from $C_L$ during a falling output transition.

$C_L = C_{ext} + C_c'$, where $C_{ext}$ is the explicit load capacitance and $C_c'$ is the effective Miller compensation capacitance reflected at the output node.

A single Miller capacitor Cc connected between the high-gain internal node (the amplifier's dominant node) and the single-ended output $v_{out}$ provides dominant-pole compensation with minimal silicon area. This Miller connection creates a dominant pole that sets the amplifier bandwidth and, if a resistor is placed in series with Cc, produces a left-half-plane (LHP) zero that can help phase margin. Proper choice of Cc and the second-stage transconductance $g_{m2}$ yields the desired gain-bandwidth product (GBW) and phase margin.

*2.6 Common Mode Rejection Ratio*

Common-Mode Rejection Ratio (CMRR) measures how well the amplifier rejects signals that are common to both inputs. In linear terms,

$$CMRR = A_d / A_{cm}, \text{ in decibels}$$

$$CMRR_{dB} = 20\log10( A_d / A_{cm} ),$$

where $A_d$ is the differential gain and $A_{cm}$ is the common-mode gainRaise differential gain $A_d$ — Telescopic cascodes (m3, m4) multiply the effective output resistance seen by the input transconductor. For the two-stage amplifier,

$$Ad \approx (g_{mb} R_{o1}) (g_{m2} R_{o2}),$$

where $g_{mb}$ is the bulk transconductance of the input pair, $R_{o1}$ is the telescopically boosted resistance at the internal node, and $g_{m2}R_{o2}$ is the second-stage gain. Increasing $R_{o1}$(via cascodes and long-L devices) directly raises $A_d$, improving CMRR.

Reduce common-mode gain $\mathbf{A_{cm}}$ — The common-mode gain is sensitive to the tail impedance and to asymmetries between branches. Using a high-impedance tail (n6 implemented as a cascode or Wilson current source) increases the tail resistance $r_{o,tail,}$ which reduces the conversion of common-mode input into differential output. Symmetric active loads (m1 = m2 with matched gates) and a balanced differential-to-single-ended converter (m5/m6) minimize systematic CM→SE conversion, shrinking $A_{cm}$.

Active Common-Mode Feedback (CMFB) — If implemented, CMFB forces the output common-mode to a stable reference and actively reduces $A_{cm}$ over DC and low frequencies; well-designed CMFB can improve CMRR by tens of dB.

*2.7 Power-Supply Rejection Ratio (PSRR)*

PSRR quantifies how much supply voltage variation appears at the amplifier output. For variations on VDD the low-frequency PSRR is typically defined as

$$PSRR_{dB} = 20\log_{10} | V_{DD} / V_{out} |$$

Cascode-biased PMOS loads (m1–m2). Driving PMOS load gates from a cascode current mirror isolates the load node from supply fluctuations. A cascode mirror increases the mirror's output resistance by roughly the cascode factor:

$$R_{out,mirror} \approx r_o(1+g_m r_o),$$

which is much larger than a simple mirror's $r_o$Because the node coupling from $V_{DD}$ to the internal nodes scales inversely with mirror output resistance, increasing $R_{out}$ reduces the fractional transfer of supply noise into the signal path, improving PSRR.

2.7 High-impedance tail and robust return path (n6, n7–n8)

For VSS perturbations, a high-impedance tail suppresses the conversion of supply (ground) ripple into common-mode currents; robust return/driver transistors prevent ground-bounce coupling to the output. Thus PSRR− is improved by a stiff tail and well-designed output return path.

Decoupling and filtering of bias nodes. Adding local decoupling capacitors on bias nodes ($V_{bias}$_cas, mirror references) and low-pass filtering reduces high-frequency coupling from supply into bias networks, improving PSRR over mid–high frequencies.

Quantitatively, making the mirror cascode changes its small-signal output resistance roughly from $r_o$ to $r_o(g_m r_o)$ often giving +8∼15 dB PSRR at low/mid frequencies.

## III. Simulation and Verification Results

The proposed bulk-driven OTA with telescopic cascode differential pair was designed and simulated using Tanner T-Spice (45 nm). The frequency response and stability behavior were evaluated under a 2.5 V supply with a 5pF compensation capacitor.

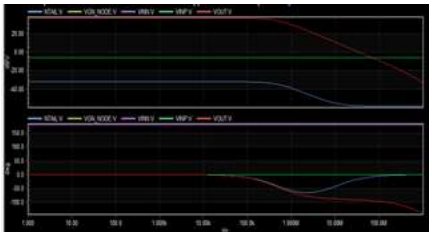

Fig. 3.1 Bode magnitude and phase response of the amplifier

Fig. 3.1 presents the Bode magnitude and phase response of the amplifier. The OTA achieves a low-frequency DC gain of approximately 48 dB, with the gain beginning to roll off near the unity-gain frequency. The measured Gain-Bandwidth Product (GBW) is about 2.7 MHz**,** and the phase margin remains within 70°**,** ensuring stable operation under all loading conditions.

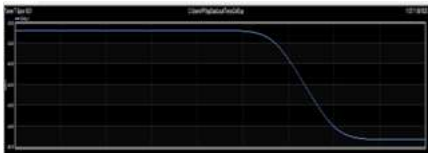

Fig. 3.2 Frequency response of the tail current source node



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Fig. 3.2 shows the frequency response of the tail current source node. The tail current maintains high impedance at low frequencies, which contributes to an improved Common-Mode Rejection Ratio (CMRR). However, at higher frequencies, the impedance decreases, limiting rejection capability.

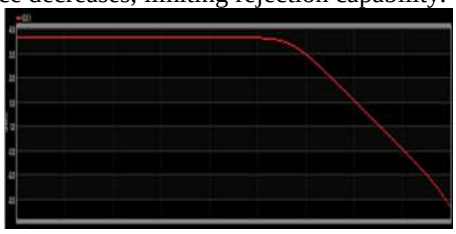

Fig. 3.3 Output magnitude response at $V_{out}$

Fig. 3.3 illustrates the output magnitude response at $V_{out}$. The OTA provides a steady DC gain at low frequency, with a sharp roll-off beyond the dominant pole. The simulated results confirm that the use of telescopic cascodes with bulk-driven input pair significantly enhances the PSRR and CMRR performance while maintaining low power operation.

| Ref | [7] | This Work |
|---|---|---|
| Year | 2022 | 2025 |
| Tech(nm) | 65 | 45 |
| Op. mode | BD | BD |
| Stages | 3 | 2 |
| Dc gain(dB) | 38 | 40 |
| GBW(MHz) | 1.65 - 0.81 | 2.5- 3 |
| Phase margin(deg) | 70.3 - 71.3 | 70 - 75 |

Table. 1 Summary of measured performance metrics and comparison with other

## IV. Conclusion

The proposed bulk-driven OTA with telescopic cascode architecture has demonstrated encouraging results in terms of gain, stability, and noise immunity; however, several opportunities for further enhancement remain open. A key direction is technology scaling, where implementing the design in advanced CMOS nodes such as 28 nm, 14 nm, or FD-SOI could significantly reduce silicon area and power consumption while enabling higher frequency operation. At the same time, scaling introduces challenges such as short-channel effects and leakage, which would require carefully optimized biasing techniques and robust layout strategies. Another important area of research is noise optimization, particularly for biomedical applications that must process extremely low signal amplitudes. Advanced techniques such as chopper stabilization, auto-zeroing, or the use of bulk-driven folded Cascode structures can help suppress flicker noise and improve signal fidelity. Furthermore, adaptive biasing strategies may be adopted to dynamically adjust current consumption based on input signal levels. This approach would minimize quiescent power during idle periods and extend the battery life of wearable and implantable biomedical devices.

## V. References

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